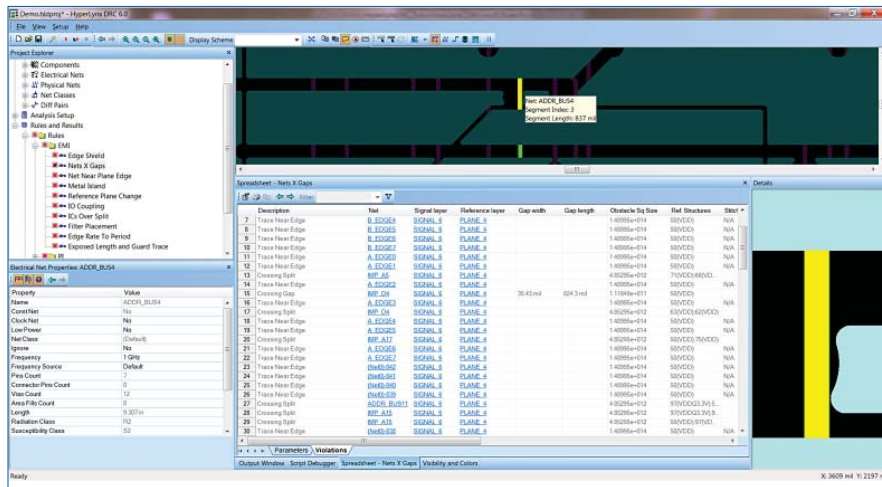


HyperLynx DRC



HyperLynx DRC performs Design Rule Checks on boards for EMI/EMC issues, as well as Signal Integrity and Power Integrity. It is highly customizable, allowing users to create DRCs for practically anything.

Overview

HyperLynx DRC is a powerful, fast design rule checking tool that is fully customizable. It allows for verification of complex design rules that are not easily simulated, such as rules for EMI/EMC. With 23 standard Design Rule Checks (DRCs) for items such as traces crossing splits, reference plane changes, shielding and via checks, you can quickly and easily pinpoint trouble spots on your board that can cause issues with EMI/EMC, Signal Integrity, and Power Integrity.

HyperLynx DRC accesses database objects through the Automation Object Model, or AOM, and allows for advanced geometrical operations on these objects. This gives you unique access to the design database and allows you to develop many types of DRCs. With support for VBScript and JavaScript, as well as thorough documentation of the AOM and DRC coding standards, and a built-in script debugging environment, you can be writing your own DRCs immediately.

Custom Rule Creation

With HyperLynx DRC, you can write custom Design Rule Checks (DRCs) which can then be run in the HyperLynx DRC by yourself and others. HyperLynx DRC contains a complete custom DRC creation environment, including a script debugger with geometry visualization.

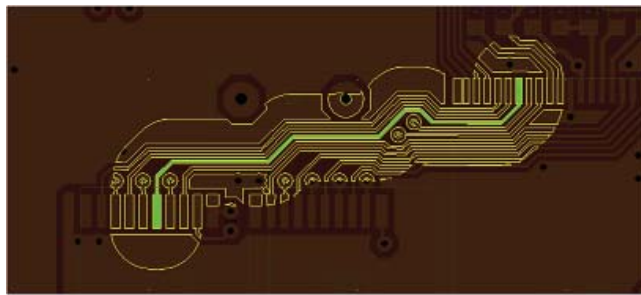
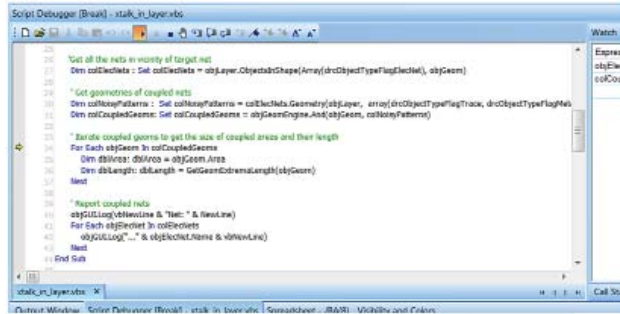
When writing custom DRCs, you can access all aspects of the layout, including stackup, layers, planes, traces, vias, pins, and TieLegs. These objects are all part of the Automation Object Model (AOM) library, which is extensively documented. The library contains the building blocks of any custom DRC. Additionally, you have access to electrical models such as IBIS. You can use custom DRCs to perform logical actions on design geometries, such as AND, OR, and XOR. Additionally, you can manipulate and measure the desired geometries of a design when performing a check.

FEATURES AND BENEFITS:

- 23 built-in checks for EMI/EMC, SI, and PI issues
- Advanced geometric engine for powerful and efficient design rule checking
- Easy setup and navigation with Setup Wizard and Project Explorer
- Complete custom DRC creation environment
- Built-in script debugger with geometry visualization
- Ability to access layout data and GUI, and manipulate and measure geometries of layout data in custom DRCs

Script Writing and Debugging Environment

HyperLynx DRC features a complete script writing and debugging environment. Built into the GUI is a script debugger, which allows you to set break points, walk through the script step by step, and add variables to a watch list. Variables on the watch list can be a variety of data, including numbers as well as geometries being operated upon by the script, which can be visualized in the board viewer in the GUI.



The script debugging environment allows you to visualize geometries being accessed by the script as you are working on your custom DRC.

Easy Setup and Navigation

The HyperLynx DRC GUI is designed for quick and easy access to design data. A built-in Setup Wizard walks you through the setup to run design checks on your board. Items such as electrical model assignment, connector definition, power/ground net definition, discrete components, and electrical net definition are all in the Setup Wizard. If you are using an Xpedition design, most of this information is already set up in Constraint Manager and transferred during the export to HyperLynx DRC. You can

review all aspects of the design using Project Explorer, which provides the navigation for the HyperLynx DRC GUI.

23 Built-In DRCs

HyperLynx DRC includes 23 standard Design Rule Checks (DRCs) which check for items related to electromagnetic interference (EMI), Signal Integrity (SI), and Power Integrity (PI). Many of the checks look for items that cannot be easily simulated, such as traces crossing splits, reference plane changes, shielding and via checks. The checks can be used to perform a comprehensive review of a board design, and eliminate problems.

Error Reports

You can select errors from the violation listing for viewing in HyperLynx DRC. In addition, Sharelist reports (containing the image, violation details and coordinates) can be generated in HTML format for broader team review.

Violation types - impedance matching for set of differential nets

Severity	Net1	Net2	Layer	Out of Impedance Length	Min Impedance	Max Impedance	Priority	Status	Plane	Plane Name	Net Parameters	U.S. Coordinates	Screenshot
Info	Differential Impedance	Differential Impedance	DIFF_2_0104	17.14 215.6	17.14 Ohm	215.6 Ohm	High	Pass	DIFF_2_0104	DIFF_2_0104	DIFF_2_0104	17.14 215.6	
Info	Differential Impedance	Differential Impedance	DIFF_2_0114	17.14 215.6	17.14 Ohm	215.6 Ohm	High	Pass	DIFF_2_0114	DIFF_2_0114	DIFF_2_0114	17.14 215.6	
Info	Differential Impedance	Differential Impedance	DIFF_2_0117	17.14 215.6	17.14 Ohm	215.6 Ohm	High	Pass	DIFF_2_0117	DIFF_2_0117	DIFF_2_0117	17.14 215.6	
Info	Differential Impedance	Differential Impedance	DIFF_2_0128	17.14 215.6	17.14 Ohm	215.6 Ohm	High	Pass	DIFF_2_0128	DIFF_2_0128	DIFF_2_0128	17.14 215.6	

Spreadsheet - Diff Impedance

Filter	Description	Rule name	Net1	Net2	Layer	Out of impedance Length	Min Impedance
1	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0D	DDR2 CLK L0D	SEGNAL_5	131.7 mil	107.94 Ohm
2	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0A	DDR2 CLK L0A	SEGNAL_5	3.258 in	107.94 Ohm
3	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0A	DDR2 CLK L0A	SEGNAL_4	1.816 in	110.7 Ohm
4	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0A	DDR2 CLK L0A	SEGNAL_4	227.1 mil	110.7 Ohm
5	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0B	DDR2 CLK L0B	SEGNAL_4	1.129 in	110.7 Ohm
6	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0C	DDR2 CLK L0C	SEGNAL_4	143.8 mil	110.7 Ohm
7	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0D	DDR2 CLK L0D	SEGNAL_4	3.275 in	110.7 Ohm
8	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0E	DDR2 CLK L0E	SEGNAL_5	38 mil	110.7 Ohm
9	Below target imp.	Rules/SD/DFI Imp.	DDR2 CLK H0F	DDR2 CLK L0F	SEGNAL_4	186.5 mil	110.7 Ohm

Supported PCB layout systems:

- Mentor PADS® Layout, Xpedition® and Board Station®
- Cadence Allegro, SPECCTRA and OrCAD Layout
- Zuken CADStar, Visula and CR3000/5000 PWS or Board Designer

For the latest product information, call us or visit: www.mentor.com/hyperlynx

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