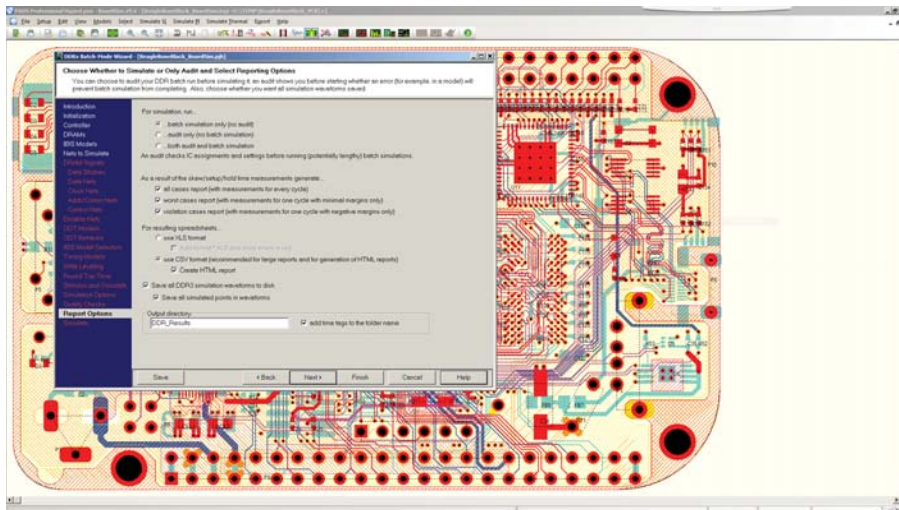




## PADS HyperLynx DDR Option

### For PADS Standard and PADS Standard Plus



The simple wizard-based interface makes it easy to set up DDR1/2/3 simulations.

#### MAJOR BENEFITS:

- Wizard-based interface helps analyze DDR1, DDR2, and DDR3 designs, including low-power variants
- Simulate with any number of DRAM devices, from single-memory to multiple-memory modules/slots
- Characterize Signal Integrity (SI) and system-level timing with setup/hold and derating calculations per JEDEC or custom standards
- Includes an HTML-based report with details of timing and SI results
- Allows an offline interactive view of simulation data

#### OVERVIEW

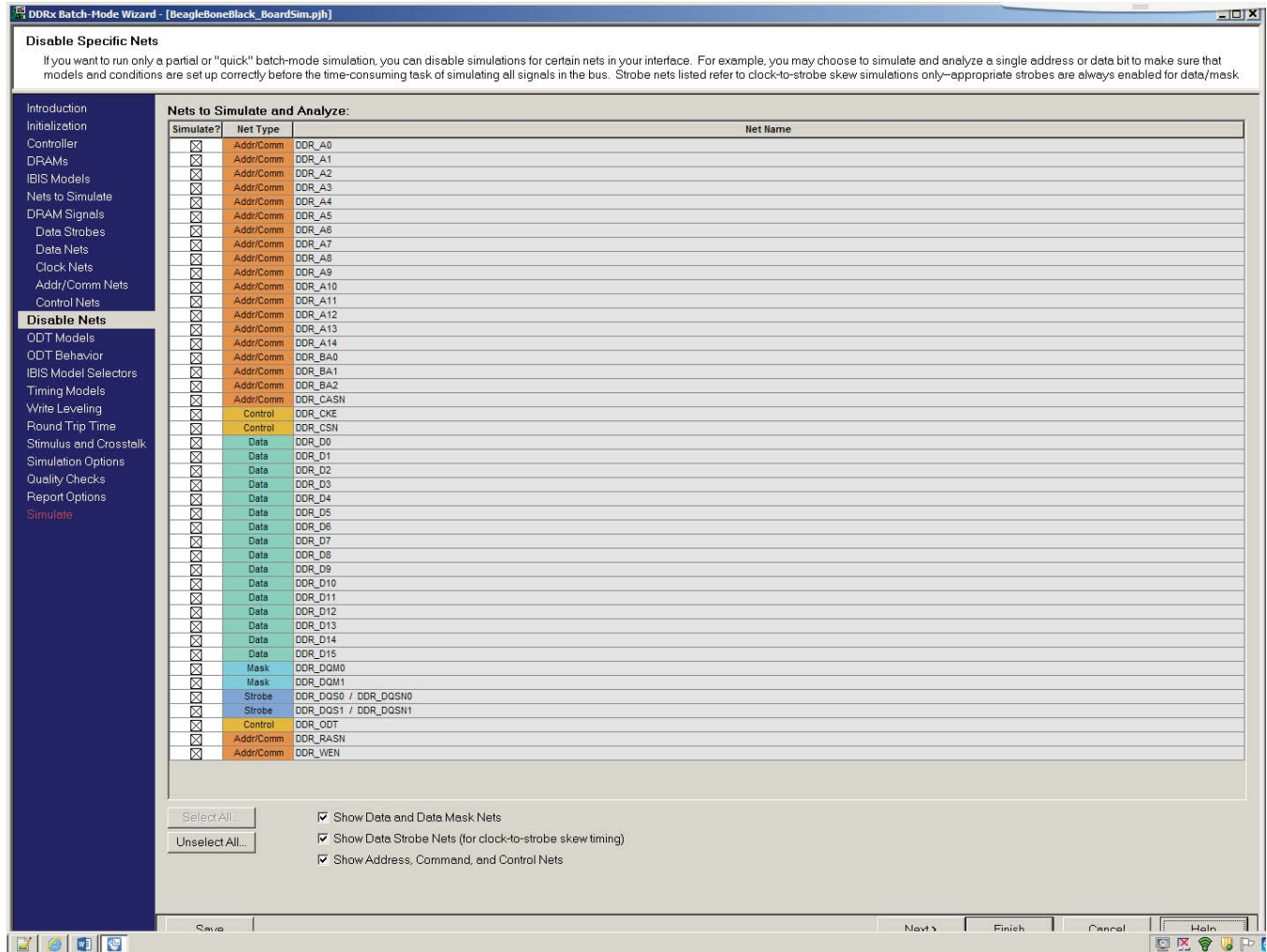
The PADS HyperLynx DDR option provides powerful analysis for PCBs with DDR memory, greatly reducing validation and debug cycles. Easily report setup/hold times, overshoot/undershoot, and non-monotonicity in your DDR interface to improve design quality. Measurements can be validated against JEDEC DDR1/2/3 standard values or custom operating points. The detailed simulations take into account board-level effects, such as lossy transmission lines, reflections, impedance changes, effects of vias, ISI, crosstalk, and timing delays, providing a comprehensive view of your memory interface.

## Easy Setup with DDRx Wizard

The HyperLynx DDRx Wizard prompts you with all the key questions necessary to set up simulations, from the simplest DDR designs to the most complicated. Users answer relevant information from a choice of IBIS models for controller and memory devices to drive-strength

values for read/write cycles, On-Die-Termination (ODT) settings, and byte-lane / strobe / mask assignment.

Wizard configurations can be saved and recalled for future use, allowing you and your team to create templates to simulate exactly what you want and to be able to re-use your setups for future designs.



Extensive options in the DDRx Wizard give you flexibility in configuring a DDR simulation.

## HTML-based Reports

The DDRx Wizard generates a clean, intuitive report at the end of the simulation process, including pass/fail data, per the information in your wizard-based configuration. Results can be filtered, letting you explore both timing and SI

concerns across data read/write cycles, on the address/command bus, or by differential nets. All results in the report are hyperlinked to the relevant simulation data to quickly launch a graphical waveform viewer for the signal(s) in question.

HyperLynx<sup>®</sup> DDR Simulation Report - DDR\_Results\_May-14-2016\_3h-37m

Data Read

Data Read Worstcases

#	Signal	Accessed DRAM	Status	Corner	Setup Margin [ns]	Hold Margin [ns]
1	DDR_D0	U12 E3	Pass	Slow	206.200	64.600
2	DDR_D1	U12 F7	Pass	Slow	194.700	68.000
3	DDR_D10	U12 C8	Pass	Slow	260.800	16.600
4	DDR_D11	U12 C2	Pass	Slow	243.600	16.600
5	DDR_D12	U12 A7	Pass	Slow	244.300	16.200
6	DDR_D13	U12 A2	Pass	Slow	237.700	39.000
7	DDR_D14	U12 B8	Pass	Slow	238.000	24.000
8	DDR_D15	U12 A3	Fail	Slow	305.900	-21.700
9	DDR_D2	U12 F2	Pass	Slow	270.800	11.400
10	DDR_D3	U12 F8	Pass	Slow	233.200	44.900
11	DDR_D4	U12 H0	Pass	Slow	224.700	45.900
12	DDR_D5	U12 H8	Pass	Slow	193.900	74.300
13	DDR_D6	U12 G2	Pass	Slow	217.400	66.000
14	DDR_D7	U12 H7	Pass	Slow	206.800	64.400
15	DDR_D8	U12 D7	Fail	Slow	310.800	-29.400
16	DDR_D9	U12 C3	Pass	Slow	258.800	19.600
17	DDR_D0	U12 E3	Pass	Fast	199.800	119.000
18	DDR_D1	U12 F7	Pass	Fast	186.900	120.000

An HTML report makes it easy to intuitively examine results and spot failures. Data can be exported in a variety of formats, according to your needs.



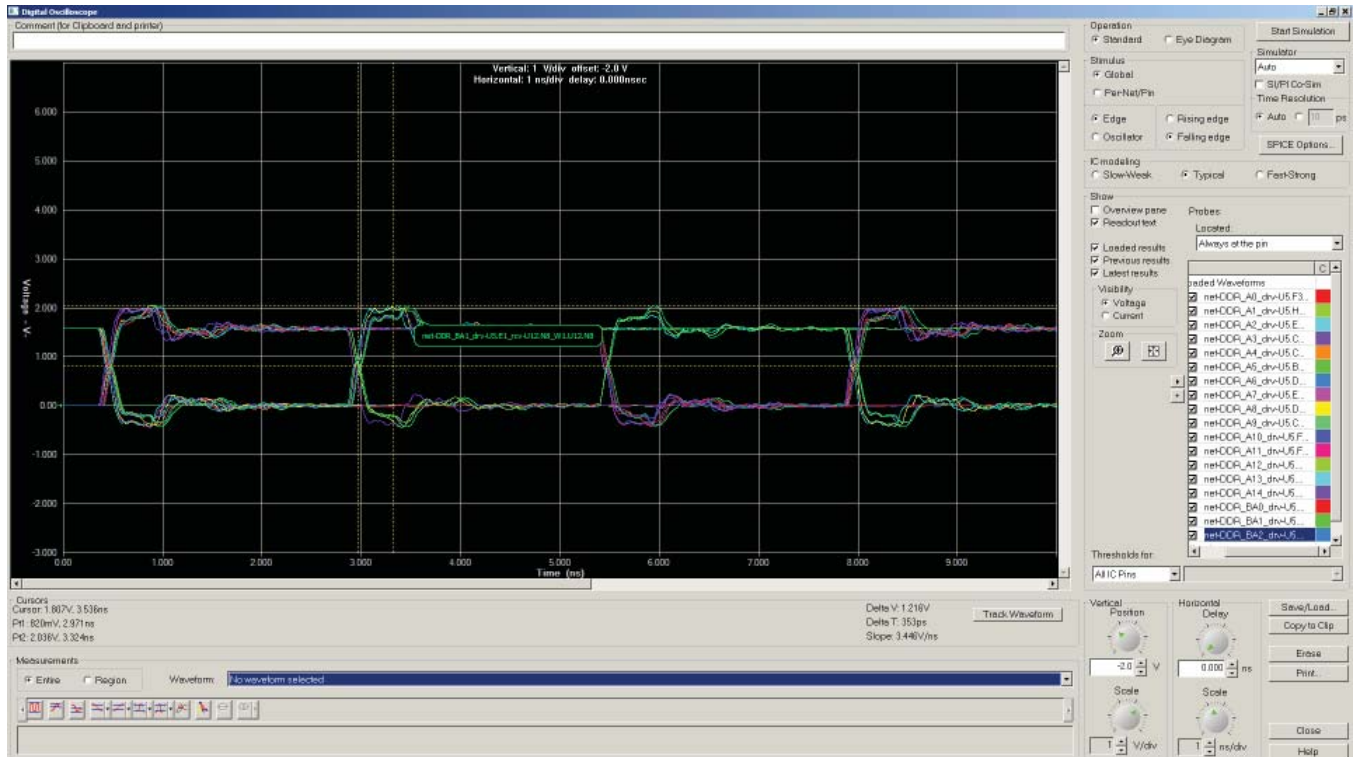
All signals in the simulation results report are hyperlinked and can show a graphical view of the signal.

## Detailed, Interactive SI analysis

Batch-mode simulation data created by the DDRx wizard can be saved to disk, so users can examine several nets simultaneously for detailed SI problems offline, using the HyperLynx oscilloscope. Users can interactively place cursors and take notes of overshoot, undershoot or signal timing.

## Summary

DDRx bus validation involves the analysis of several timing and voltage measurements. Manual analysis of an entire DDR bus is impractical and error prone. HyperLynx DDRx greatly reduces the setup time required for a successful simulations\ while providing detailed results that can help drive decisions in your design process.



Load any number of signals from batch-mode results into an interactive oscilloscope to take detailed measurements.

For the latest product information, call us or visit: [www.pads.com](http://www.pads.com)

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